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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,720	12/31/2001	Doug Larson	ADTST.043AUS	2220

7590 07/13/2004

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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,720	LARSON ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-8 are presented for examination.

Specification

1. The disclosure is objected to because of the following informalities:

a. Page 4 line 30 recites, "means for stroking an output" but the examiner believes it should read "means for strobing an output".

b. Page 5 line 5 recites, "stroking the output" but the examiner believes it should read "strobing the output".

c. Page 8 line 15 recites, "resolution of equal" but the examiner believes it should read, "resolution equal".

d. Page 11 line 13 recites, "shifted its time" but the examiner believes it should read, "shifted in time".

e. Page 12 line 25 recites, "terming vernier" but the examiner believes it should read, "timing vernier".

Appropriate correction is required.

Claim Objections

2. Claim 5 is objected to because of the following informalities: the word "stroking" appears 2 times, but the examiner believes it should be "strobing". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 6 recites the limitation "the multiplexer" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Yoshiba, U.S. Patent No. 6253360. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131. Yoshiba teaches, in a prior art drawing, a time shift circuit for a semiconductor test system for changing a delay timing of a portion of a test pattern for

testing a semiconductor device (see Abstract), comprising: a multiplexer (FIG.5 27) for selectively producing delay value data indicating a value of time shift (FIG.5 RATDAT) for a specific portion of test pattern in response to a shift command signal (FIG.5 MT); a vernier delay unit (FIG.5 22) for producing timing vernier data based on programmed delay data prepared in the semiconductor test system (FIG.5 21) and the delay value data selected by the multiplexer (FIG.5 27); and a timing generator (FIG.5 14) for generating a timing edge for the specific portion of the test pattern (+ or – as per FIG.5 PTND) based on the timing vernier data from the vernier delay unit (output of FIG.5 22); wherein the shift command signal (FIG.5 MT) sets either a normal mode (FIG.5 CLDAT) where predetermined delay value data is selected by the multiplexer (FIG.5 27A) or a time shift mode (FIG.5 CLDAT and RATDAT) where delay value data for shifting the timing edge in real time is selected by the multiplexer (FIG.5 27B).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being obvious over Yoshiba, U.S. Patent No. 6253360, as applied to Claim 1 above, and in view of Sugamori, U.S. Patent No. 6172544. The applied reference has a common assignee with the instant

application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2). ***

As per Claim 2:

Yoshiba fails to further teach the time shift circuit as defined in claim 1, wherein the vernier delay unit comprises an adder. But in an analogous art, Sugamori does teach an adder (FIG.2 35-39) for summing the programmed delay data and the selected delay value data (column 8 lines 27-31); a decoder for decoding higher bits of output data of the adder to produce a register select signal (FIG.2 35); and a series of delay registers for delaying the timing vernier data configured by lower bits of the output data

of the adder where one of the delay registers is selected by the register select signal to receive the timing vernier data as a first delay register (FIG.2 +0, +1, +2, or +3). And the advantage of Sugamori, a timing circuit with high resolution and simplicity of design, is stated in column 2 lines 55-68. One with ordinary skill in the art at the time of the invention, motivated to improve Yoshiba, would combine the timing generator of Sugamori at the multiplexer output of Yoshiba, and would find it to be an obvious improvement to Yoshiba.

As per Claim 3:

Sugamori further teaches the time shift circuit as defined in claim 2, wherein the timing vernier data (FIG.2 +0, +1, +2, or +3) is shifted in the series of delay registers (FIG.2 41, 43, 45, 47) starting from the first delay register at each clock (FIG.2 CLK2), thereby producing the timing vernier data (FIG.2 51) at a timing which is an integer multiple of a clock period. And in view of the motivation previously stated, the claim is rejected.

As per Claim 4:

Yoshia, in Claim 1, fails to teach a fine delay based on less than one cycle of the clock. But Sugamori does teach this feature; a time shift circuit as defined in claim 1, wherein the timing generator (FIG.2) includes a fine delay circuit (FIG.2 all but 15) for receiving the timing vernier from the vernier delay (FIG.2 SELECT 1, 2) unit and producing a delay time which is smaller than one cycle of the clock (FIG.2 CLK1) based on the timing vernier data. The circuit clock, CLK2, is 4x the base clock, CLK1, and

therefore the maximum vernier falls within one CLK1 cycle. And in view of the motivation previously stated, the claim is rejected.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being obvious over Yoshiba, U.S. Patent No. 6253360, and in view of Goto et al., U.S. Patent No. 5712855. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2). Yoshiba teaches, in a prior art drawing, a time shift circuit for a semiconductor test system for changing a delay timing of a portion of a test pattern for testing a semiconductor device (see Abstract), comprising: a vernier delay unit (FIG.5

22) for producing timing vernier data based on programmed delay data prepared in the semiconductor test system (FIG.5 21) and the delay value data selected from a counter (FIG.5 27); and a timing generator (FIG.5 14) for generating a timing edge for the specific portion of the test pattern (+ or – as per FIG.5 PTND) based on the timing vernier data from the vernier delay unit (output of FIG.5 22), and based also on a mode signal (FIG.5 MT). Yoshiba however fails to teach a counter that increments delay data to determine timing for an output signal strobe circuit wherein the counting is controlled by the state of the output signal. But in an analogous art, this feature is taught. Goto et al. teaches a counter for transferring delay value data in a normal mode and incrementing the delay value data in an AC parametric measurement mode to determine a delay timing of a portion of the test pattern applied to a device under test where a mode selection signal selects either the normal mode or the AC parametric measurement mode (FIG.1 and column 4 lines 8-60); and means for strobing an output signal of the device under test at the timing edge from the timing generator (FIG.1 7); and a strobe recovery circuit for determining pass or fail status of the output signal of the device under test and producing a fail signal when the output signal fails(FIG.1 73); wherein the fail signal is provided to the counter during the AC parametric measurement mode to increment the delay value data (column 4 lines 20-25), thereby continuously shifting the timing edge for strobing the output signal of the device under test until a change of state in the output signal is detected (column 4 lines 20-25). The advantage of Goto et al., as in column 1 lines 15-65), is a system that can quickly test circuit timing without recursive applications of pattern data. And one with ordinary skill in the art at the

time of the invention, motivated as suggested would find it obvious to join the references together at the multiplexer of Yoshiba in order to perform a quick and accurate test of DUT circuit delay.

7. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being obvious over Yoshiba, U.S. Patent No. 6253360, and in view of Goto et al., U.S. Patent No. 5712855, as applied to Claim 5 above, and further in view of Sugamori, U.S. Patent No. 6172544. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2). ***

As per Claim 6:

Yoshiba and Goto et al. fail to further teach the time shift circuit as defined in claim 5, wherein the vernier delay unit comprises an adder. But in an analogous art, Sugamori does teach an adder (FIG.2 35-39) for summing the programmed delay data and the selected delay value data (column 8 lines 27-31); a decoder for decoding higher bits of output data of the adder to produce a register select signal (FIG.2 35); and a series of delay registers for delaying the timing vernier data configured by lower bits of the output data of the adder where one of the delay registers is selected by the register select signal to receive the timing vernier data as a first delay register (FIG.2 +0, +1, +2, or +3). And the advantage of Sugamori, a timing circuit with high resolution and simplicity of design, is stated in column 2 lines 55-68. One with ordinary skill in the art at the time of the invention, motivated to improve Yoshiba, would combine the timing generator of Sugamori at the multiplexer output of Yoshiba, and would find it to be an obvious improvement to Yoshiba.

As per Claim 7:

Sugamori further teaches the time shift circuit as defined in claim 6, wherein the timing vernier data (FIG.2 +0, +1, +2, or +3) is shifted in the series of delay registers (FIG.2 41, 43, 45, 47) starting from the first delay register at each clock (FIG.2 CLK2), thereby producing the timing vernier data (FIG.2 51) at a timing which is an integer multiple of a clock period. And in view of the motivation previously stated, the claim is rejected.

As per Claim 8:

Yoshia and Goto et al., in Claim 5, fail to teach a fine delay based on less than one cycle of the clock. But Sugamori does teach this feature; a time shift circuit as defined in claim 1, wherein the timing generator (FIG.2) includes a fine delay circuit (FIG.2 all but 15) for receiving the timing vernier from the vernier delay (FIG.2 SELECT 1, 2) unit and producing a delay time which is smaller than one cycle of the clock (FIG.2 CLK1) based on the timing vernier data. The circuit clock, CLK2, is 4x the base clock, CLK1, and therefore the maximum vernier falls within one CLK1 cycle. And in view of the motivation previously stated, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Guy J. Lamarre
for
Albert DeCady
Primary Examiner